Potential Induced Degradation of solar cells and panels

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ABSTRACT: This paper is focusing on Potential Induced Degradation (PID) of wafer based standard p-type silicon technology once exposed to external potentials in the field. Test setups are presented for simulation of the PID in the lab and the influence of cell properties on PID is demonstrated in order to reveal the cell being the precondition for the PID. However, the solar cells need to be exposed to High Voltage Stress (HVS) caused by a negative potential relative to ground in order to potentially cause any relevant PID in the field within the 25 years life time of a solar panel. Besides the key parameters on cell level the paper is also presenting options on panel and system level in order to prevent PID and therefore to further decrease overall degradation rates of PV systems. Moreover, the impact of climatic conditions as temperature and humidity on the extent of PID was also investigated and results are presented in the paper.
Keywords: Degradation, Reliability, Performance

1 INTRODUCTION

Since solar energy generation is getting more and more important worldwide PV systems and solar parks are becoming larger consisting of an increasing number of solar panels being serially interconnected. As a consequence panels are frequently exposed to high potentials relative to ground causing High Voltage Stress (HVS). The potential impact of voltage-biased humidity exposure of solar panels on long term stability was first addressed by Hoffman and Ross in 1978 [1] and studies on the effect of HVS on long term stability of solar panels depending on the leakage current between solar cells and ground have been published by NREL in 2005 [2]. However, until now the degradation mechanism correlated with HVS is not covered by the standard test procedures listed in IEC 61215 [3].

Depending on the technology different types of Potential Induced Degradation (PID) occur. The most prominent case for PID in silicon solar cell technology is Sunpower's polarization effect [5] but also other technologies like a-Si and ribbon silicon have been reported in the past to be prone to different types of PID under certain circumstances – either reversible e.g. polarization or irreversible e.g. electro chemical corrosion [4]. All known PID effects have one common characteristic: The degradation is depending on polarity and level/extent of the potential between cell and ground which is determined by the actual configuration of the PV system.

Up to now very different standards exist concerning the configuration of PV systems. Whereas in Europe PV systems are certified for voltages up to 1000V, in the US only 600V are allowed according to NEC. Additionally there are different regulations in respect to grounding for different countries and districts. As a consequence the market access for transformer less inverters technologies which are very common in Europe is very restricted in the US since according to NEC solid grounding of the PV system is still the standard configuration.

However, there are intensive efforts being made in order to achieve common standards aiming on 1000V as maximum system voltage and the change of grounding regulations in the US.

Whereas increasing system voltages and the introduction of transformer less inverters certainly have a positive impact on the overall cost efficiency of solar parks, it has to be put into account that on the same time solar panels are exposed to increasing HVS within solar systems. So investigating PID for standard silicon cells can not only avoid significant power degradation in future systems. It also can be considered as a clear track for the reduction of the overall degradation of a panel is therefore a suitable method in order to expand the life time of a solar panel even further.

2 OBJECTIVE

The focus of this paper is to present suitable methods for measuring the PID on panel level as well as showing possibilities to minimize/avoid PID on cell, panel and system level.
It shall be demonstrated that although the precondition for PID can be located at cell level it is the combination of several parameters such as high potential relative to ground, panel layout and environmental factors such as humidity and temperature which are impacting the extent of power degradation in the field within a panel's life time.

3 EXPERIMENTAL

3.1 PID setup for full size panels:

For the simulation of worst case scenarios in the field two different accelerated test methods were applied in order to measure PID on panel level.
In figure 1 the general setup is presented showing the maximum negative voltage relative to ground in the field being simulated by the application of a potential (1000 V) between the frame and the positive pole of the panel. In order to increase the leakage current the glass surface is covered with a constant and continuous water film realized by a sprinkler. A stack set up was used in order to study the impact of solar cell properties and panel layout on the PID stability of up to 16 panels in parallel.

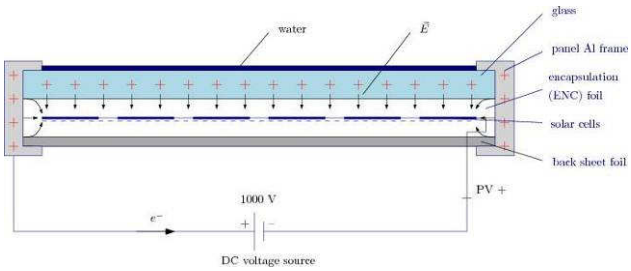

Figure 1: Principal test setup for PID measuremnts

For the investigation of the impact of environmental factors single panels biased according to figure 1 were placed in the climatic chamber in order to control humidity and temperature.

3.2 PID setup for single-cell-laminates

For studying the impact of cell properties on PID single cell laminates (see **Figure 2**) were built and HVS was caused by applying - 1000 V to one of the cell poles. The positive pole of the power supply is connected to a wet blanket touching the sunny side of the single cell laminate.

Figure 2: Single-cell-laminates

3.3 Standard test procedure for PID

For characterization of the cells and panels prior and after the PID test an IV curve as well as a high resolution electroluminescence (EL) image were captured.
The standard PID test was run for 100h.
To investigate the leakage currents from cell to ground an ampere meter with data logger was used.

4 BACKGROUND AND APPROACH

In order to better understand the factors impacting PID the three different levels – cell, panel and system – were separately investigated.

4.1 Cell level

The cell was found to be the precondition for PID. Some process steps as well as the quality of the base material have been identified to significantly contribute to the extent of PID tendency on cell level. In the result chapter we take a closer look at the different cell parameters influencing the PID.

4.2 Panel level

Environmental factors such as humidity and temperature [2] as well as the panel design are influencing leakage currents within the panel. The impact of humidity and temperature is presented in **Figure 3**.

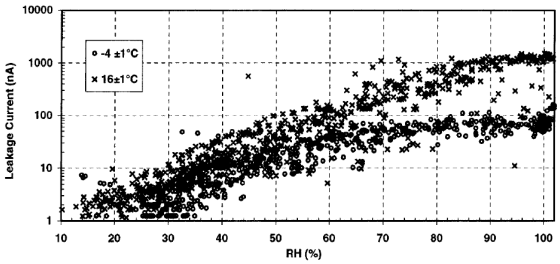

Figure 3: Dependency of panel leakage current on temperature and humidity [2]

In case of solar cells being prone to PID high leakage currents on panel level support PID. The interaction of the different panel materials is resulting in certain leakage current paths which are illustrated in **Figure 4**. According to Mc Mahon et al [8] the leakage current path Ip2 is dominating the others.
Higher leakage currents can be caused by water (vapor) entering the solar panel causing the encapsulation (ENC) material becoming more conductive.

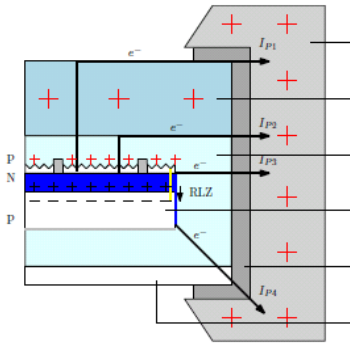

Figure 4: Leakage currents paths within a solar panel according to Mc Mahon et al [8]

As a consequence panel design and layout can impact the leakage currents and therefore play a role for the HV-durability of panels.

4.3 System level

On system level the potential difference between ground and cell is the most important factor for PID. The system voltage depends in first order on the number of panels serially interconnected and the irradiation and in second order on the panel temperature.
The final potential of a cell relative to ground is determined by the grounding configuration. Depending on the negative, positive or no pole being grounded the resulting potential the cell is exposed to relative to ground is either fixed at a certain positive or negative value or it is not fixed – called floating potential. In the latter case one part of the string has a negative and the other a positive potential relative to ground.

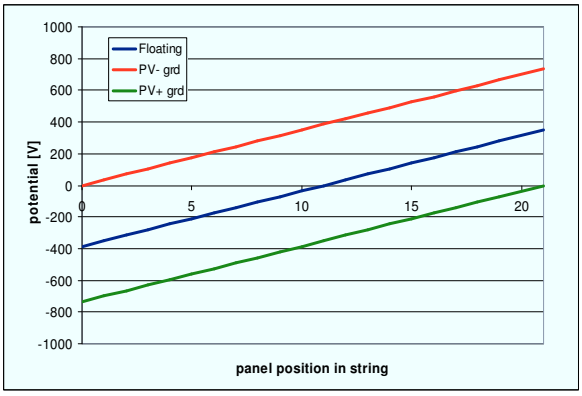

Figure 5: Potential in a string, different grounding schemes PV+/PV- and no grounding (floating potential)

5 RESULTS

5.1 Cell level

The following two graphs show the evolution of the IV curve for a solar cell prone to PID and the corresponding power degradation over time.

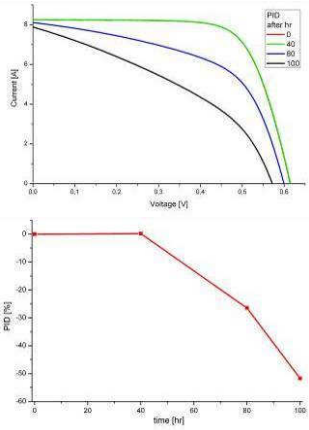

Figure 6: Evolution of the IV curve and the corresponding power with progressing PID

As illustrated in
Table 1 in case of PID shunt resistance as well as the reverse bias current are affected first followed by FF. Finally the open circuit voltage decreases reflecting the junction to be less capable of separating holes and electrons.

t	Uoc	Isc	P	FF	I (-12V)	Rsh
[hr]	[V]	[A]	[W]	%	[A]	[Ω]
0	0,615	8,240	3,61	71,4	0,21	80,4
20	0,619	8,261	3,66	71,5	0,22	80,4
40	0,615	8,258	3,62	71,3	0,30	51,1
80	0,600	8,109	2,65	54,6	>10	0,5
100	0,572	7,882	1,74	38,7	>10	0,2
rel. PID	-7%	-4%	-52%	-46%	-	-100%

Table 1: Cell IV key parameter change by PID

The Isc is the parameter that is least affected but with advancing PID Isc also degrades. Depending on the degree of PID the junction is loosing its blocking characteristic under reverse bias eventually being short cutted (ohmic shunt). This phenomenon can be visualized by EL images taken during a PID test shown in the upper row of **Figure 7**. After 40hr local shunts appear along the edge of the cell that degrade further from diode to ohmic behavior, as can be seen in the reverse bias image in the lower row of **Figure 7**. First shunted areas appear bright but after further PID evolution these areas do not emit any more breakdown light [6]. Finally after 100hr both images are dark because of dominating ohmic shunts.

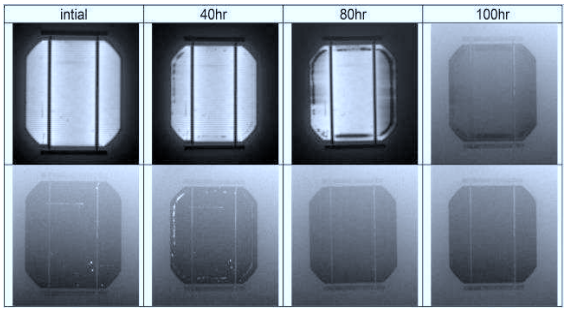

Figure 7: EL image of a cell during PID test (upper row) and the corresponding reverse bias (-12V) image (lower row)

The leakage current within the panel is resulting in a certain charge concentration above the solar cell in the ENC. Depending on certain cell properties these charges might interact with the emitter and the depletion layer finally causing shunting of the cell. From semiconductor industry similar effects are known as (time dependent) dielectric breakdown or surface inversion [5]. The electric field of these charge carriers is influencing the p-n-junction in that way that the junction gets more conductive and the local shunt resistance drops.
There are numerous factors on cell level being important in respect to PID. In the following we present the parameters identified to have the most significant impact.

5.1.1 Anti-reflective coating

There are different parameters having an large impact on PID but the ARC deposition was shown to have a crucial role in not only influencing but actually preventing PID on cell level.
In case of typical standard cells ARC is realized by SiNx applied by a various deposition technologies resulting in a certain thickness layer thickness and refractive index (RI) determining the specific properties of the layer.
Figure 8 is illustrating the huge impact of parameter variations for the ARC deposition on the extent on PID. It also shows that by using suitable combination of RI and thickness PID can be completely prevented on cell level.

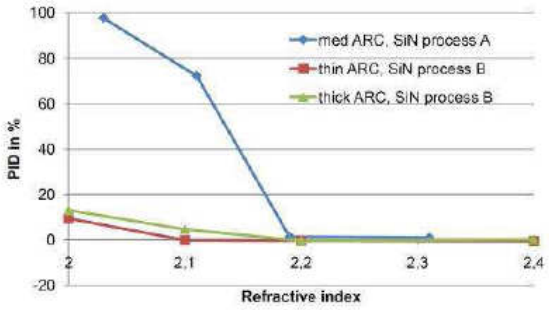

Figure 8: Dependency of PID on SiN RI and thickness.

For ARC deposition the third parameter having an impact on PID was found to be the homogeneity of the resulting SiN layer which was recognized to be clearly different for various SiN deposition methods.
The observations made for the role of the SiN parameter concerning PID can be explained by the different conductivity of the resulting layer for different parameter settings making trapping of charges more or less likely.

5.1.2 Wafer material

Also the wafer material has been identified to be another crucial factor regarding PID. The most significant parameter in this respect is the base resistivity. As presented in **Figure 9** an increasing base resistivity is resulting in decreasing PID. Higher base resistivity representing lower base doping leads to a wider depletion layer at the junction when the emitter doping is held constant. Accordingly shunting of the junction is less likely.

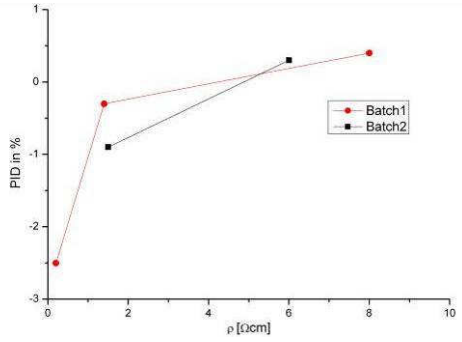

Figure 9: Dependency of PID on base resistivity

Within different experiments with cell suppliers where cells have been produced at constant cell processing parameters utilizing different wafer suppliers a significant batch dependence has been found. This could hint on systematic variation of certain wafer properties relevant for PID.
Lower quality silicon or comparably high concentration of crystal defects seem to increase the tendency of PID but results have to be further verified.

5.1.3 Emitter

Since the emitter process clearly influences the width of the depletion layer it can definitely be influencing the probability for shunting the PN-junction and therefore the tendency for PID. As it can be seen in **Figure 10** with increasing emitter sheet resistivity PID is also increasing.

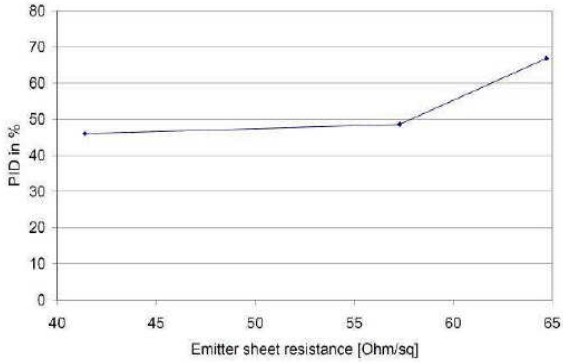

Figure 10: Dependency of PID on emitter sheet resistance.

Beside the trend in solar industry to increase the emitter sheet resistivity for solar cells it can be additionally increased by new process steps such as emitter back etching or the introduction of the selective emitter process.
This example shows that process variations within the cell process which are thought to be of no relevance for the later application can lead to degradation when the cell are exposed to an external potential later in the field.
Since there are many factors on cell level impacting PID there is no easy distinction between cells more or less prone to PID just by IV characterization. However, due to the PID mechanism and the impacting factors discussed above there are some IV characteristics that hint on lower PID sensitivity: high shunt resistance and low reverse bias current. Both parameters are depending on local defects and base resistivity.
According to our recent results the most effective path for prevention of PID on cell level is the selection of suitable parameters (RI and thickness) for ARC deposition.

5.2 Panel level

Since PID is not yet completely excluded on cell level for all industrial solar cells being produced today it is certainly worthwhile to take a closer look on the possibilities to minimize or exclude PID on the panel level even in case of solar cells prone to PID. In **Figure 11** there are shown EL images for a solar panel before and after the PID test (1000V, 100hr).
According to the image after the test some cells degrade strongly - finally being short circuited - while others appear to be stable. Being the cell the origin for PID this observation can be explained by variation of certain cell properties relevant for PID as discussed in the chapter above.

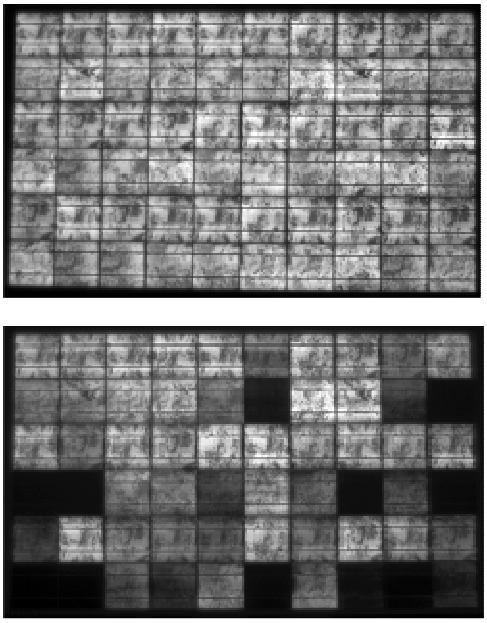

Figure 11: EL image of a panel before (upper) and after (lower) 100hr 1000V PID test

The findings in the EL images do match the observed power drop of about 30% found after the PID test.

The objective was to investigate how PID on panel level can be influenced by the panel layout or design. Different material combinations have been checked in respect to whether or not the PID is rather supported or suppressed. It turned out that an important factor is the type of ENC material since the leakage current can be influenced. In the following figure the leakage current is shown as a function of time during a temperature ramp up from -20°C to 48°C in a humid atmosphere (50% RH). According to **Figure 12** two different encapsulation materials are causing the peak leakage current to differ by more than one order of magnitude. The panel can be described here as a capacitor being charged while the temperature is rising. When finally the full capacity is reached the current will drop again.

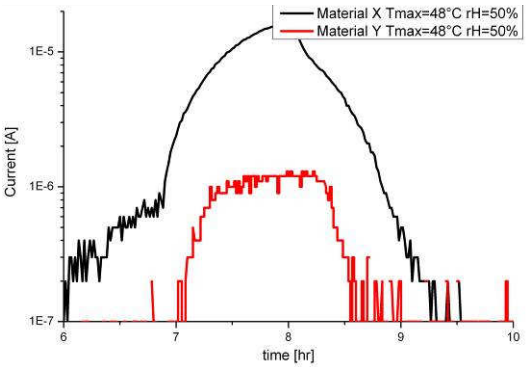

Figure 12: Leakage current for two panels with different ENC materials during a temperature ramp from -20°C to 48°C with 1000V applied voltage (RH 50%).

As a consequence of this significant difference in leakage current the PID results with varying ENC materials differ strongly as shown in **Figure 13.**

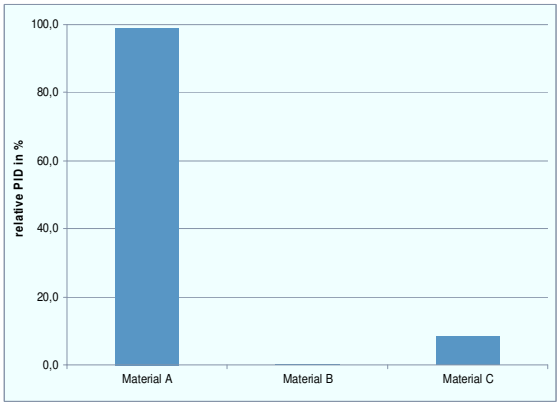

Figure 13: PID comparison of three different ENC materials in panels with prone solar cells

Since leakage current on panel level seems to be the key feature for suppressing PID on panel level it was also investigated how it is influenced by different environmental factors such as temperature and moisture. In the Arrhenius plot in **Figure 14** it can be seen both increasing temperature (T-ramp from -20 °C to 85°C) and increasing humidity (0% versus 50%) resulting in higher leakage currents.

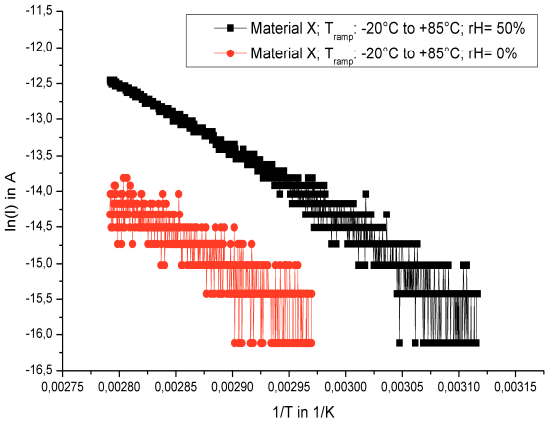

Figure 14: Arrhenius plot for the leakage current depending on temperature and humidity during PID test (1000V, 100h).

The leakage current for the two test panels in this test being exposed to different levels of relative humidity (RH) also corresponds to the different extent of power degradation (Table 2) obtained for different RH.

Material combination	Conditions	Δ P in%
Material x	T= 85°C; RH=0%	- 10
Material x	T= 85°C; RH=50%	- 32
Material x	T= 85°C; RH=100%	- 99

Table 2: Power drop of three panels (same layout) after PID test (1000V, 100h, in climatic chamber running a T ramp -20°C to 85°C) being exposed to different RH.

Even if temperatures and humidity according to **Table 2** are meant to be a worst case scenario they show very impressively the potential impact of environmental

factors on PID.

In order to minimize or avoid PID on panel level and therefore to increase life time and reliability suitable material combinations and panel design have to be found to ensure low leakage currents. In this case PID can be successfully suppressed even for panels with solar cells prone to PID.
Using PID suppressing encapsulation materials is one of the layout options in this matter. There are alternative materials to standard EVA better performing in respect to PID but other criteria like price, handling, long term stability issues and availability have to be taken into account.

5.3 System level

As already mentioned one precondition for PID is the existence of HVS which is very much influenced by the specific system configuration – mainly by the kind of grounding. As already shown in Figure 5 the kind of grounding determines the potential relative to ground a panel is exposed to which is also changing with panel position within a string.
In absence of grounding resulting in a so called *floating potential* there is only one part of the string being exposed to a negative potential causing HVS potentially turning into PID.
The higher the negative potential the panel is exposed to the higher the extent of PID as illustrated by corresponding EL images of a string within a floating system in **Figure 15**.

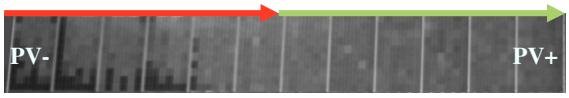

Figure 15: EL image of a PID affected string of a floating test system. Only the panels marked by the red arrow are exposed to a negative potential relative to ground and therefore prone to PID.

Therefore avoiding negative potential relative to ground is one way for p-type standard cells on system level in order to minimize PID independent on cell and panel properties. This could be achieved by grounding the negative pole of the system. However, this is not always possible since in the last few years inverter technologies have been widely introduced particularly in Europe which do not allow the grounding of the negative pole due to the absence of transformers.

Nevertheless, it could be shown that PID cannot only be prevented on system level by avoiding negative potential it could also been shown that PID can even be recovered by reversing the potential having caused the PID. By showing the reversibility of the PID effect (provided electrochemical corrosion is excluded) recovery methods could be developed for affected panels as well as systems in order to reverse the power loss caused by PID.

The reversibility of PID for solar panels has been demonstrated in the lab on PID affected panels by applying the reverse potential in respect to the one originally causing PID. Whereas for standard like solar panels the recovery has been done by applying a positive potential as shown in **Figure 16**, for other technologies like Sunpower's back contact technology it was already found in 2005 that the *polarization effect* [4] can be reversed by applying a negative potential.

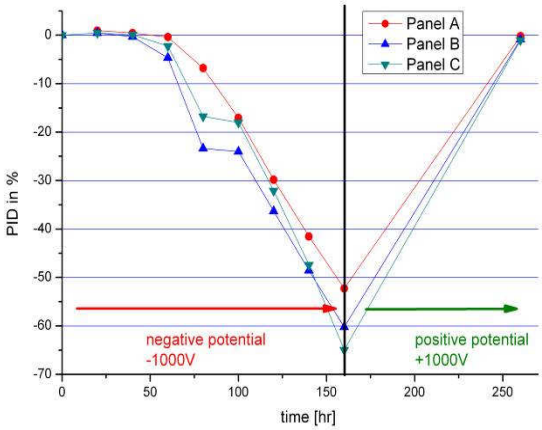

Figure 16: Degradation and recovery of panels in the lab by reversing the applied potential

As a consequence grounding of the positive pole of the PV system or even a potential shift towards positive potential as illustrated in **Figure 17** can not only prevent PID on system level it also supports the regeneration of the panels which is demonstrated in **Figure 18**.

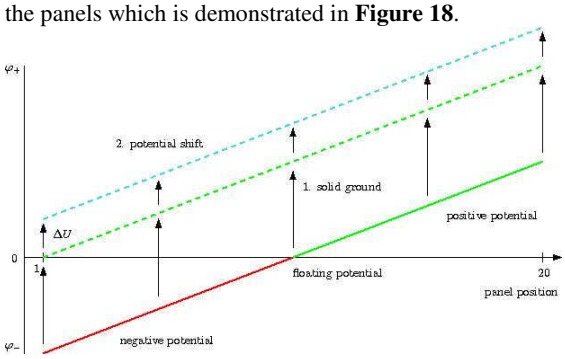

Figure 17: System configurations supporting the recovery of PID (solid ground or potential shift) versus floating potential.

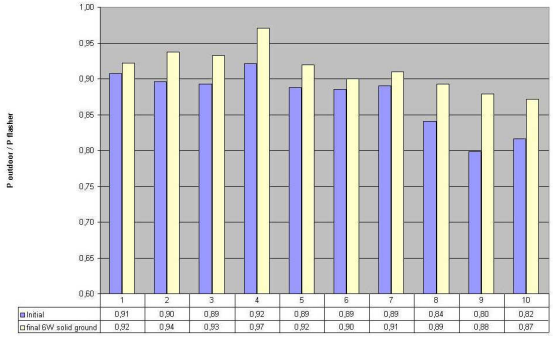

Figure 18: Regeneration of a test string with PID affected panels by solid grounding of the negative pole

The time necessary for the recovery process depends not only on the potential but – analog to the degradation process - also on environmental factors such as humidity and temperature.

6 SUMMARY AND CONCLUSION

This paper addressed a degradation mechanism called Potential Induced Degradation (PID) that is believed to get increasing importance with growing PV systems and corresponding higher system voltages. Moreover, there will be an increasing need for further reduction of overall degradation rates for PV system in order to make PV systems even more profitable on the long term.
Summarizing all parameters supporting PID it has to be concluded that there are four main factors to be taken into account:
First the precondition is a solar cell prone to PID.
Second there has to be a panel layout not systemically suppressing PID by particularly low leakage currents.
Third the panel has to be exposed to a negative potential relative to ground.
Fourth the outer conditions have to be additionally support high leakage currents as comparably high moisture and temperatures.
Being aware of these main factors it was explained that - although the origin of PID is on cell level – it can be minimized or avoided on all levels – system, panel and cell. The solution on system level is simply the avoidance of negative potential by choosing suitable grounding of the system. However, it has been suggested that also high positive potentials relative to ground can cause degradation as electrochemical corrosion [9].
This makes a solution on cell or panel level even more favorable.
On panel level leakage current was identified to be the main feature to keep as low as possible by a suitable panel layout and design.
On cell level many parameters influence the PID stability of solar cells but the most important parameter is found to be the ARC deposition since by choosing of suitable parameter settings PID can be banned on cell level. This would be an enormous advantage since the system approach by grounding is not always feasible due to the use of transformer less inverters especially in Europe.

Taking these findings into account long term stability of solar panels can be significantly improved by adapting processes on all levels in order to minimize PID and therefore optimize the energy output of the PV system over a 25 years life time.

7 OUTLOOK

The scenarios investigated with laboratory and outdoor tests are simulating worst case conditions with high humidity and constantly high voltage. At SOLON an experiment is going on directly comparing laboratory results with outdoor data at the different SOLON test sites (Germany, US and Italy) covering also the impact of different environmental conditions.

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